Notice of Allowability	Application No. 10/815,559	Applicant(s) BALL, JAMES LORAN	
	Examiner Paul W. Schlie	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *an examiner initiated interview and resulting amendment dated 8/3/06 and 8/10/06*.
2. ☒ The allowed claim(s) is/are *1-3 and 6-30*.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
   1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Godfrey Kwan on 8/3/06 and 8/10/06, whereby:

Claims 1, 8, 12-13, 16-17, 20, 24-26, 28-30 are amended; and

Claims 4-5 are canceled.

3. The application has been amended as follows:

1. (Currently Amended) A processor, comprising:

a plurality of registers;

processing circuitry associated with the plurality of registers, wherein the processing circuitry is operable to execute instructions included in a supported instruction set;

an instruction cache coupled to the processing circuitry, wherein the instruction cache is configured to provide copies of instructions in memory to the processing circuitry, the instruction cache including a first subset of instruction cache lines and a second subset of instruction cache lines, the second subset of instruction cache lines including one or more cache lines not included in the first subset;

wherein a first subset of instruction cache lines are invalidated using reset address line invalidate circuitry upon reset without using bypass circuitry, the first subset of instruction cache lines corresponding to instructions in memory used to invalidate the second subset of instruction cache lines.

~~reset address line associated with the instruction cache is invalidated using reset address line invalidate circuitry upon reset.~~

2. (Original) The processor of claim 1, wherein reset address line invalidate circuitry invalidates a single line in instruction cache upon reset.

3. (Original) The processor of claim 1, wherein each line in the instruction cache comprises a tag portion and an instruction portion.

4. (Canceled)

5. (Canceled)

6. (Original) The processor of claim 5, wherein the tag portion includes the state of an instruction cache line.

7. (Original) The processor of claim 5, wherein the processor further comprises a data cache.

8. (Currently Amended) The processor of claim 7, wherein instructions copied comprise instructions for invalidating the second subset of instruction cache lines.~~all other lines in the instruction cache.~~

9. (Original) The processor of claim 7, wherein instructions copied comprise instructions for invalidating all lines in the data cache.

10. (Original) The processor of claim 1, wherein the processor is a processor core on a programmable chip.

11. (Original) The processor of claim 10, wherein the processor is coupled to memory through a simultaneous multiple primary component fabric.

12. (Currently Amended) The processor of claim 10, wherein the processor can have its instruction cache invalidated and its data cache invalidated upon reset without the use of bypass circuitry.

13. (Currently Amended) A programmable chip system, comprising:

processing circuitry associated with a plurality of registers, wherein the processing circuitry is operable to execute instructions included in a supported instruction set, the processing circuitry associated with reset address line invalidate circuitry operable to invalidate a first subset of cache lines upon reset without using bypass circuitry, the first subset of cache lines corresponding to instructions in memory used to invalidate a second subset of cache lines, the second subset of instruction cache lines including one or more cache lines not included in the first subset;~~a line in processor cache;~~

a plurality of components coupled to the processing circuitry through an interconnection module.

14. (Original) The programmable chip system of claim 13, wherein reset address line invalidate circuitry invalidates a single line in instruction cache upon reset.

15. (Original) The programmable chip system of claim 13, wherein each line in the instruction cache comprises a tag portion and an instruction portion.

16. (Currently Amended) The programmable chip system of claim 15, wherein invalidating the first subset of instruction cache lines ~~reset address line~~ associated with the instruction cache comprises setting the tag portion of the first subset of instruction cache lines ~~reset address line~~ to invalid.

17. (Currently Amended) The programmable chip system of claim 16, wherein instructions from memory are copied into the instruction cache at the reset address line upon identifying that the first subset of instruction cache lines have been invalidated~~the invalid state of the reset address line~~.

18. (Original) The programmable chip system of claim 17, wherein the tag portion includes the state of an instruction cache line.

19. (Original) The programmable chip system of claim 17, wherein the programmable chip system further comprises a data cache.

20. (Currently Amended) The programmable chip system of claim 19, wherein instructions copied comprise instructions for invalidating the second subset of cache lines.~~all other lines in the instruction cache.~~

21. (Original) The programmable chip system of claim 19, wherein instructions copied comprise instructions for invalidating all lines in the data cache.

22. (Original) The programmable chip system of claim 13, wherein the interconnection module is a simultaneous multiple primary component fabric.

23. (Original) The programmable chip system of claim 22, wherein the processor can have its instruction cache invalidated upon reset without the use of bypass circuitry.

24. (Currently Amended) A method for performing a reset, the method comprising:

identifying a reset event at a processor;

invalidating a ~~reset address line associated with a processor cache;~~ first subset of cache lines associated with processor cache without the use of bypass circuitry upon identifying the reset event, the first subset of cache lines corresponding to a plurality of instructions in memory used to invalidate a second subset of cache lines, the second subset of instruction cache lines including one or more cache lines not included in the first subset;;

obtaining ~~a~~ the plurality of instructions from memory, the plurality of instructions obtained after a read access request for the first subset of cache lines~~the reset address line~~;

executing ~~a~~ the plurality ~~sequence~~ of instructions to invalidate a plurality of lines associated with the processor cache.

25. (Currently Amended) The method of claim 24~~1~~, wherein the first subset of cache lines are ~~reset address line is~~ associated with a processor instruction cache.

26. (Currently Amended) The method of claim 24~~1~~, wherein the plurality ~~sequence~~ of instructions invalidates substantially all of the lines associated with processor cache.

27. (Original) The method of claim 1, wherein reset events are associated with hardware faults and software faults.

28. (Currently Amended) A processor, comprising:

means for identifying a reset event;

means for invalidating a ~~reset address line associated with a processor cache;~~ first subset of cache lines associated with processor cache without the use of bypass circuitry upon identifying the reset event, the first subset of cache lines corresponding to a plurality of instructions in memory used to invalidate a

second subset of cache lines, the second subset of instruction cache lines including one or more cache lines not included in the first subset;

means for obtaining ~~a~~ the plurality of instructions from memory, the plurality of instructions obtained after a read access request for the first subset of cache lines~~the reset address line~~;

means for executing ~~a~~ the plurality ~~sequence~~ of instructions to invalidate a plurality of lines associated with the processor cache.

29. (Currently Amended) The processor of claim 28, wherein the first subset of cache lines are ~~reset address line is~~ associated with a processor instruction cache.

30. (Currently Amended) The processor of claim 28, wherein the plurality ~~sequence~~ of instructions invalidates substantially all of the lines associated with processor cache.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul W. Schlie whose telephone number is 571-272-6765. The examiner can normally be reached on Mon-Thu 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 517-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PIERRE BATAILLE
PRIMARY EXAMINER
8/11/06